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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Bruno GHYSELEN et al.	Confirmation No.: 8095
Patent No.: 6,953,736 B2	Application No.: 10/615,259
Patent Date: October 11, 2005	Filing Date: July 9, 2003
For: PROCESS FOR TRANSFERRING A LAYER OF STRAINED SEMICONDUCTOR MATERIAL	Attorney Docket No.: 4717-7500

REQUEST FOR CERTIFICATE OF CORRECTION UNDER 37 C.F.R. § 1.322

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

Patentees hereby respectfully request the issuance of a Certificate of Correction in connection with the above-identified patent. The corrections are listed on the attached Form PTO-1050. The corrections requested are as follows:

On the title page, before Item (51), insert the following:

-- (30) **Foreign Application Priority Data**

Jul. 9, 2002 (FR) ..... 02 08602 --

Priority of French Application No. 02 08602 filed July 9, 2002 was made on applicants' Declaration filed on October 30, 2003. The certified priority document was filed on July 22, 2005 to perfect applicants' claim. Thus, it respectfully is requested that the foreign application priority data be added by way of Certificate of Correction.

At column 16, line 66 (claim 23, line 2), after "The method of claim", delete "**21**" and insert -- **22** --. Support for this change appears in application claim 28.

At column 17, line 1 (claim 24, line 1), after "The method of claim **23**", insert -- wherein --. Support for this change appears in application claim 29.

The requested corrections are for errors that appear to have been made by the Office. Therefore, no fee is believed to be due for this request. Should any fees be required, however, please charge such fees to Winston & Strawn LLP Deposit Account No. 50-1814. Please issue a Certificate of Correction in due course.

Respectfully submitted,

10/26/05
Date

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212-294-3311

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,953,736 B2
DATED: October 11, 2005
INVENTORS: Ghyselen et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page:
Before Item (51), insert the following:
-- (30) **Foreign Application Priority Data**
Jul. 9, 2002 (FR) ..... 02 08602 --.

Column 16:
Line 66, after "The method of claim", delete "**21**" and insert -- **22** --.

Column 17
Line 1, after "The method of claim **23**", insert -- wherein --.

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US00[redacted]3736B2

(12) **United States Patent**
Ghyselen et al.

(10) **Patent No.: US 6,953,736 B2**
(45) **Date of Patent: Oct. 11, 2005**

(54) **PROCESS FOR TRANSFERRING A LAYER OF STRAINED SEMICONDUCTOR MATERIAL**

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(73) Assignee: **S.O.I.Tec Silicon on Insulator Technologies S.A.**, Bernin (FR)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **10/615,259**

(22) Filed: **Jul. 9, 2003**

(65) **Prior Publication Data**

US 2004/0053477 A1 Mar. 18, 2004

Related U.S. Application Data

(60) Provisional application No. 60/445,825, filed on Feb. 10, 2003.

(51) **Int. Cl.**[7] **H01L 21/30**

(52) **U.S. Cl.** **438/458**; 438/478

(58) **Field of Search** 438/458, 460

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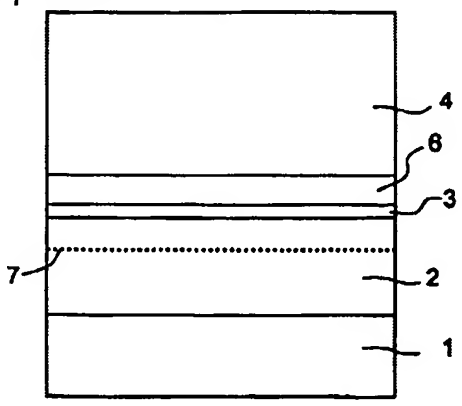
(57) **ABSTRACT**

The invention relates to a process for producing an electronic structure that includes a thin layer of strained semiconductor material from a donor wafer. The donor wafer has a lattice parameter matching layer that includes an upper layer of a semiconductor material having a first lattice parameter and a film of semiconductor material having a second, nominal, lattice parameter that is substantially different from the first lattice parameter and that is strained by the matching layer. This process includes transfer of the film to a receiving substrate. The invention also relates to the semiconductor structures that can be produced by the process.

26 Claims, 9 Drawing Sheets

(30) Foreign Application Priority Data
Jul. 9, 2002 FR 0208602



Preferably, the strained layer of this embodiment is of silicon and the oxide is silica. When these materials are used, the critical thickness of the strained layer, which is the thickness beyond which the layer relaxes and defects can typically appear in the crystalline structure of the layer, can be significantly increased. This consequently permits a thicker strained layer to be produced than can be produced with the strained silicon being associated directly with silicon germanium. The strained silicon layer can be thickened by growing to achieve a thickness of around 60 nm. Preferably, the strained silicon layer is thickened by growing to a thickness of between about 40 nm and 60 nm.

While illustrative embodiments of the invention are disclosed herein, it will be appreciated that numerous modifications and other embodiments may be devised by those skilled in the art. For example, while in the preferred embodiment a strained silicon film **3** in transferred, other types of films of a semiconductor able to be strained and transferred can be transferred according to a process of the invention. Additionally, in the semiconductor layers, other constituents may be added thereto, such as carbon with a carbon concentration in the layer in question of less than or equal to about 50% or more preferably with a concentration of less than or equal to about 5%. Therefore, it will be understood that the appended claims are intended to cover all such modifications and embodiments that come within the spirit and scope of the present invention.

What is claimed is:

1. A method of preparing a semiconductor wafer, which comprises:

providing a matching substrate that comprises a handling substrate and a matching layer on the handling substrate, the matching layer having a first lattice parameter on a first surface disposed opposite the handling substrate, and the handling substrate having a second lattice parameter that is different from the first lattice parameter;

creating a region of weakness in the matching layer, wherein the region of weakness is configured to facilitate splitting;

growing on the first surface of the matching layer a first strained layer of a first semiconductor material in a strained state to impart the same first lattice parameter in the first strained layer as in the matching layer;

associating a receiving substrate with the first strained layer to form a composite structure;

obtaining a product wafer and a donor wafer by splitting the composite structure at the region of weakness, wherein the product wafer includes the strained first layer and the receiving substrate and a retained portion of the matching layer on the first strained layer, while the donor wafer includes at least a portion of the matching layer;

smoothing roughness from the retained portion of the matching layer; and

selectively etching the smoothed portion of the matching layer from the first strained layer.

2. The method of claim **1**, wherein the matching layer includes a buffer layer and a relaxed surface layer on which the first strained layer is grown.

3. The method of claim **2**, wherein the lattice parameter of the buffer layer is graded between the first and second lattice parameters.

4. The method of claim **1**, wherein the region of weakness is created by implanting atomic species.

5. The method of claim **1**, wherein the region of weakness is created by adding a porous layer.

6. The method of claim **1**, wherein the lattice parameter of the first material when strained is different than the lattice parameter of the first material in a relaxed state.

7. The method of claim **1**, wherein the receiving substrate is bonded to the first strained layer.

8. The method of claim **1**, wherein the first strained layer is disposed directly adjacent an insulator on a side of the first strained layer on which the receiving substrate is disposed.

9. The method of claim **1**, wherein the first strained layer comprises silicon, and the matching layer comprises silicon germanium.

10. The method of claim **1**, wherein the region of weakness is formed after the growing the first strained layer.

11. The method of claim **1**, wherein the first strained layer is strained for modifying the energy band structure of the semiconductor material of that layer for improving the electrical properties thereof compared to the semiconductor material in a relaxed state.

12. The method of claim **11**, wherein the first strained layer has a thickness that is less than the critical thickness thereof for preventing substantial relaxation of strain.

13. The method of claim **12**, wherein first strained layer has a thickness of less than about 20 nanometers prior to the splitting.

14. The method of claim **11**, wherein the first strained layer has a charge carrier mobility that is at least about 50% higher than in the semiconductor material in a relaxed state.

15. The method of claim **1**, further comprising providing a first strain-retaining layer on the first strained layer for maintaining strain from the side of the first strained layer opposite the matching layer.

16. The method of claim **15**, wherein the first strain-retaining layer has the first lattice parameter.

17. The method of claim **16**, wherein the matching and first strain-retaining layers are made of substantially the same material.

18. The method of claim **15**, growing a second strained layer of semiconductor material on the first strain-retaining layer to impart the first lattice parameter therein.

19. The method of claim **18**, further comprising providing a second strain-retaining layer on the second strained layer and having the first lattice parameter for maintaining the strained state of the second strained layer from the side of the second strained layer opposite the first strain-retaining layer.

20. The method of claim **18**, further comprising:

providing a region of weakness in the first strain-retaining layer;

transferring a second layer to a second receiving substrate by splitting at the region of weakness in the first strain-retaining layer; and

transferring the first strained layer to a first receiving substrate.

21. The method of claim **15**, wherein:

the first strained layer comprises first material; and

the first strain retaining layer comprises an oxide of the first material.

22. The method of claim **15**, wherein the first strained layer comprises silicon and the first strain-retaining layer comprises silica, and the method further comprising associating the first strain-retaining layer with the silicon of the first strained layer prior to the splitting.

23. The method of claim **21**, further comprising thickening the strained layer of silicon epitaxially after the splitting.

22

Wherein

24. The method of claim 23, the strained layer is thickened epitaxially after the splitting to a layer thickness of greater than about 40 nm.

25. A method of preparing a semiconductor wafer, comprising:

providing a matching layer, which has a first lattice parameter on a first surface of the matching layer, on a handling substrate, which has a second lattice parameter that is different from the first lattice parameter;

growing on the first surface of the matching layer a first strained layer of a first semiconductor material in a strained state to impart the same first lattice parameter in the first strained layer as in the matching layer;

associating a receiving substrate with the first strained layer to form a composite structure; and

transferring the first strained layer from the matching layer to the receiving substrate by splitting the matching layer from the strained layer, such that the transferred strained layer is in a strained state and a retained portion of the matching layer is retained on the strained layer; and

smoothing roughness from the retained portion of the matching layer; and

selectively etching the smoothed portion of the matching layer from the strained layer.

26. The method of claim 1, wherein the first strained layer of the product wafer in a strained state.

* * * * *